Amendments to the Specification

Please replace the paragraph beginning on page 14, line 11 with the following amended paragraph:

Described next with reference to Fig. 6 is detailed configurations of the operational amplifiers 501 and 502. Fig. 6 is a circuit diagram showing each configuration of the operational amplifiers 501 and 502. Meanwhile, the operational amplifiers 501 and 502 have the same configuration. The operational amplifiers 501 and 502 each comprises a PMOS transistor P61 which operates in response to the signal /test, a PMOS transistor P62 which operates in response to a signal inputted to the noninverting input terminal (+terminal), a PMOS transistor P63 which operates in response to a signal inputted to the inverting input terminal (-terminal), an NMOS transistor N61 which operates in response to the signal /test, and NMOS transistors N62 and N63 constituting a current mirror circuit. A gate (control electrode) of the PMOS transistor P61 is connected to the control terminal DIS, a source (first electrode) thereof is connected to a power supply node to which the power supply voltage VDD is supplied, a drain (second electrode) thereof is connected to the PMOS transistors P62 and P63. A gate (control electrode) of the PMOS transistor P62 is connected to the noninverting input terminal (+terminal), a source (first electrode) thereof is connected to the drain of the PMOS transistor P61, a drain (second electrode) thereof is connected to the NMOS transistors N61, N62 and N63. A gate (control electrode) of the PMOS transistor P63 is connected to the inverting input terminal (-terminal), a source (first

electrode) thereof is connected to the drain of the PMOS transistor P61, a drain (second electrode) thereof is connected to an output terminal OUT. A gate (control electrode) of the NMOS transistor N61 is connected to the control terminal DIS, a source (first electrode) thereof is connected to the ground voltage node to which the ground voltage GND is supplied, and a drain (second electrode) thereof is connected to the drain of the PMOS transistor P62. A gate (control electrode) and a drain (second electrode) of the NMOS transistor N62 are connected in common to each other, and a source (first electrode) thereof is connected to the ground voltage node. A gate (control electrode) of the NMOS transistor N63 is connected to the gate of the NMOS transistor N62, a source (first electrode) thereof is connected to the ground voltage node, and a drain (second electrode) thereof is connected to the output terminal OUT. The NMOS transistors N62 and N63 constitute a current mirror circuit wherein the NMOS transistor N62 is positioned at an input side of the current mirror circuit and the NMOS transistor N63 is positioned at an output side thereof. A common connection node between the drain of the PMOS transistor P62 [[P61]], the drain of the NMOS transistors N61 and the drain of the NMOS transistor N62 is defined as n1.

Please replace the paragraph beginning on page 18, line 20 with the following amended paragraph:

An input terminal of the inverter circuit INV71 is connected to a test terminal 101 via a test control signal line test, and an output terminal thereof is connected to the

operational amplifier 701 and the NMOS transistor N12. A gate (control electrode) of the NMOS transistor N71 is connected to the test terminal 101 via the test control signal line test, a first electrode thereof is connected to an input terminal 102 via an input signal line in, and a second electrode thereof is connected to an internal circuit 112. The internal circuit 112 is a circuit which is susceptible to a noise generated in a signal to be inputted thereto, e.g., an analog circuit. A noninverting input terminal (+terminal) of the operational amplifier 701 is connected to the input terminal 102 via the input signal line in, and an inverting input terminal (-terminal) and an output terminal thereof are connected in common to each other, and a common connection node thereof is connected to the internal circuit 112, and a control terminal DIS thereof is connected to the output terminal of the inverter circuit INV71 via the signal line /test. The configuration of the operational amplifier 701 is the same as that of the circuit of the operational amplifier shown in Fig. 6. A gate of the PMOS transistor P12 is connected to the test terminal 101 via the test signal line test, a first electrode thereof is connected to the input terminal 102 via the input signal line in, and a second electrode thereof is connected to the internal circuit 111. A gate of the NMOS transistor N12 is connected to an output terminal of the inverter circuit [[INV51]] INV71 via the signal line /test, a first electrode thereof is connected to the input terminal 102 via the input signal line in, and a second electrode thereof is connected to the internal circuit 111. The first electrode of the NMOS transistor N12 and the first electrode of the PMOS transistor P12 are connected in common to each other. The second electrode of the NMOS transistor

N12 and the second electrode of the PMOS transistor P12 are connected in common to each other. The internal circuit 111 is a circuit which is hardly susceptible to the noise generated in a signal to be inputted thereto, e.g., a digital circuit.

Please cancel the subparagraph on page 20, lines 16-24.

Please insert the following paragraph on page 20, after line 16:

The test mode operation is described next. The PMOS transistor P12 turns OFF in response to the test control signal test of "H". The NMOS transistor N12 turns OFF in response to the signal /test of "L". In such a manner, the connection between the input terminal 102 and the internal circuit 111 is interrupted. The NMOS transistor N71 turns ON in response to test control signal test of "H" to transmit the input signal in to the internal circuit 112. The operational amplifier 701 is active in response to the signal /test of "L" to output the output signal out _ 701 having the same level of the input signal in.

Please replace the paragraph beginning on page 20, line 25 with the following amended paragraph:

Described next is an operation in the case where there occurs an ~~undershoot~~ overshoot in the input signal in during the test mode operation. Since the power supply

voltage VDD is supplied to the gate of the NMOS transistor N71 and a voltage which is higher than the power supply voltage VDD is supplied to the first electrode thereof, the voltage of the second electrode of the NMOS transistor N71 becomes "power supply voltage VDD-Vtn", where Vtn is a threshold voltage of the NMOS transistor N71.

Please replace the paragraph beginning on page 21, line 25 with the following amended paragraph:

A switch circuit of a fifth embodiment of the invention is described. Fig. 8 is a circuit diagram showing a configuration of a switch circuit according to the fifth embodiment of the invention. The switch circuit of the fifth embodiment comprises an inverter circuit INV81 for outputting a signal /test having a phase opposite to that of a test control signal test in response to the test control signal test, a PMOS transistor P81 which operates in response to the ~~test control~~ signal /test [[test]], an operational amplifier 801 which outputs an output signal out _ 801 in response to an input signal in, a PMOS transistor P12 which operates in response to the test control signal test, and an NMOS transistor N12 which operates in response to the signal /test. The signal and a wiring for transmitting the signal are depicted by the same reference numeral.

Please replace the paragraph beginning on page 22, line 9 with the following amended paragraph:

An input terminal of the inverter circuit INV81 is connected to a test terminal

101 via a test control signal line test, and an output terminal thereof is connected to the operational amplifier 801 and the NMOS transistor N12. A gate (control electrode) of the PMOS transistor P81 is connected to ~~a test terminal 101~~ the signal /test via the ~~test control~~ signal line /test [[test]], a first electrode thereof is connected to an input terminal 102 via the input signal line in, and a second electrode thereof is connected to an internal circuit 112. The internal circuit 112 is a circuit which is susceptible to a noise generated in a signal to be inputted thereto, e.g., an analog circuit. A noninverting input terminal (+terminal) of the operational amplifier 801 is connected to the input terminal 102 via the input signal line in, and an inverting input terminal (-terminal) thereof and an output terminal thereof are connected in common to each other, and a common connection node thereof is connected to the internal circuit 112, and a control terminal DIS thereof is connected to the output terminal of the inverter circuit INV81 via the signal line /test. The configuration of the operational amplifier 801 is the same as that of the circuit of the operational amplifier shown in Fig. 6. A gate of the PMOS transistor P12 is connected to the test terminal 101 via the test signal line test, the first electrode thereof is connected to the input terminal 102 via the input signal line in, and a second electrode thereof is connected to the internal circuit 111. A gate of the NMOS transistor N12 is connected to an output terminal of the inverter circuit INV51 via the signal line /test, a first electrode thereof is connected to the input terminal 102 via input signal line in, and a second electrode thereof is connected to the internal circuit 111. The first electrode of the NMOS transistor N12 and the first electrode of the PMOS transistor

P12 are connected in common to each other. The second electrode of the NMOS transistor N12 and the second electrode of the PMOS transistor P12 are connected in common to each other. The internal circuit 111 is a circuit which is hardly susceptible to the noise generated in a signal to be inputted thereto, e.g., a digital circuit.

Please replace the paragraph beginning on page 23, line 16 with the following amended paragraph:

The normal mode operation is first described. The PMOS transistor P12 turns ON in response to the test control signal test of "L". The NMOS transistor N12 turns ON in response to the signal /test of "H". In such a manner, the input terminal 102 and the internal circuit 111 are forced into conduction. The PMOS transistor P81 turns OFF in response to the signal /test of "H". The operational amplifier 801 outputs an output signal out _ 801 of "Hi-Z" in response to the signal /test of "H". The voltage of the output signal out _ 801 is not susceptible to the voltage of the input signal in. Even if there occurred the undershoot in the input signal in during the normal mode operation so that the voltage of the input signal in was lower than the ground voltage GND, a pnp-type bipolar transistor formed in the PMOS transistor [[P71]] P81 turns OFF. Accordingly, even if there occurred the undershoot in the input signal in during the normal mode operation so that the voltage of the input signal in was lower than the ground voltage GND, a signal having a voltage which is lower than the ground voltage GND is not transmitted to the internal circuit 112.

Please replace the paragraph beginning on page 25, line 2 with the following amended paragraph:

A switch circuit of a sixth embodiment of the invention is described. Fig. 9 is a circuit diagram showing a configuration of a switch circuit according to the sixth embodiment of the invention. The switch circuit of the sixth embodiment comprises an inverter circuit INV91 for outputting a signal /test having a phase opposite to that of a test control signal test in response to the test control signal test, an operational amplifier 901 which is controlled in an operative condition in response to the signal /test and outputs an output signal out _ 901 in response to an input signal in, an NMOS transistor N91 and a PMOS transistor P12 which operate in response to the test control signal test, and a PMOS transistor P91 and an NMOS transistor N12 which operate in response to the signal /test. An input terminal of the inverter circuit INV91 is connected to a test terminal 101 via a test control signal line test, and an output terminal thereof is connected to the operational amplifier 901, the PMOS transistor P91 and the NMOS transistor N12 via the signal line /test A noninverting input terminal (+terminal) of the operational amplifier 901 is connected to an input terminal 102 via an input signal line in, and an inverting input terminal (-terminal) and an output terminal thereof are connected in common to each other, and a common connection node thereof is connected to an internal circuit 112, and a control terminal DIS thereof is connected to the output terminal of the inverter circuit INV91 via the signal line /test. The configuration of the operational amplifier 901 is the same as that of the operational

amplifier shown in Fig. 6. The internal circuit 112 is a circuit which is susceptible to a noise generated in a signal to be inputted thereto, e.g., an analog circuit. A gate (control electrode) of the NMOS transistor N91 is connected to the test terminal 101 via the test signal line test, a first electrode thereof is connected to an input terminal 102 via the input signal line in, and a second electrode thereof is connected to the PMOS transistor P91. A gate (control electrode) of the PMOS transistor P91 is connected to an output terminal of the inverter circuit INV91 via the signal line /test, a first electrode thereof is connected to the second electrode of the NMOS transistor N91, a second electrode thereof is connected to the internal circuit 112 and a substrate thereof is connected to the second electrode thereof. A gate (control electrode) of the PMOS transistor [[P91]] P12 is connected to a test terminal via the test control signal test, a first electrode thereof is connected to the input terminal 102 via the input signal line in and a second electrode thereof is connected to the internal circuit 111. A gate (control electrode) of the NMOS transistor N12 is connected to the output terminal of the inverter circuit INV91 via the signal line /test, a first electrode thereof is connected to the input terminal 102 via the input signal line in and a second electrode thereof is connected to the internal circuit 111. The first electrode of the PMOS transistor P12 and the first electrode of the NMOS transistor N12 are connected in common to each other, while the second electrode of the PMOS transistor P12 and the second electrode of the NMOS transistor N12 are connected in common to each other. The internal circuit 111 is a circuit which is hardly susceptible to the noise generated in a signal to be

inputted thereto, e.g., a digital circuit.

Please replace the paragraph beginning on page 28, line 8 with the following amended paragraph:

Described next is an operation in the case where there occurs the overshoot in the input signal in during the test mode operation. Since the power supply voltage VDD is supplied to the gate of the NMOS transistor N91, and a voltage which is higher than the power supply voltage VDD is supplied to the first electrode thereof, the voltage of the second electrode of the NMOS transistor [[N911]] N91 becomes "the power supply voltage VDD - Vtn", where Vtn is a threshold voltage of the NMOS transistor N91. A signal of "the power supply voltage VDD - Vtn" is transmitted to the internal circuit 112.

Please replace the paragraph beginning on page 28, line 23 with the following amended paragraph:

As mentioned above, the switch circuit of the sixth embodiment includes the operational amplifier 901 which is connected between the input terminal 102 and the internal circuit 112 and operates in response to the test control signal test, and the NMOS transistor [[NP91]] N91 and the PMOS transistor P91 which are connected between the input terminal 102 and the internal circuit 112 and operate in response to the test control signal test respectively, so that even if there occurred the overshoot or the undershoot in the input signal in, it is possible to prevent the signal from being

transmitted to the internal circuit 112. The switch circuit of the sixth embodiment can prevent the internal circuit 112 from being susceptible to a noise generated in the input signal in.